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Power: Die 48 Gesetze der Macht - Kindle Edition - Robert Greene. Power: Die 48 Gesetze der Macht: Kompaktausgabe Robert Greene. Power: Die 48 Gesetze der Macht. Robert Greene. 18,00 €. Power: Die 48 Gesetze der Macht: Kompaktausgabe.Interconnection systems are employed in many applications to provide connectivity among different parts of equipment. One example of an interconnection system is a data bus which provides an interface for exchanging data among a number of different systems or subsystems. A typical application for such an interconnection system is within a microprocessor system which provides bus connections among the processor, various peripheral devices (e.g., memory, display subsystem, and I/O subsystem) and other components within the microprocessor. A typical bus architecture includes a number of interconnected bus "slaves" which are connected to a number of bus "master" devices. Communication among the bus slaves and bus master devices occurs through a bus which may be either unidirectional (i.e., master-to-slave) or bidirectional (i.e., master-to-master). The data bus typically provides a "local" data bus which is a serial data bus for carrying data and address information among a group of bus slaves and a "global" data bus which is typically employed for large scale system data transfer among multiple groups of bus slaves. For example, data may be transferred on the local data bus among the bus slaves and the global data bus may be employed to transfer data among the local data buses. Typical buses provide various timing features to meet design criteria, such as communication speed, scalability, delay, reliability and density. Designing a bus system which meets all of the design criteria is a challenge. Designers of buses attempt to meet these design criteria with a combination of parallel and serial interconnection technology. Parallel technology is typically employed for high speed communication while serial interconnection is typically employed for long distance, low speed applications. One of the most significant problems with traditional bus architectures is the lack of any effective way to synchronize bus slaves. Most bus architectures rely upon some type of clock or reset signal to synchronize the bus slaves, which introduces timing problems for the bus. In a traditional bus architecture, bus slaves employ a system clock which is generated by the system. If the clock frequency is insufficient, the bus slaves may become unsynchronized. In 2d92ce491b